

**REMARKS****Allowable Subject Matter**

The Examiner is thanked for the thorough examination of this application and the allowance of claims 8-20.

Claims 1-5 and 7-21 remain in this application. Claim 1 is amended herein by replacing the term "on different planes" to "on more than one face thereof" to overcome 112 rejections. In addition, claim 1 has been amended by adding "at least two isolation substrates contact at respective substrate-combining regions". Support for the amendment is shown at least in page 6, lines 4-6, "FIGs. 5A and 5B show the circuit blocks connected by the electrical connecting elements, wherein the isolation substrates are in contact".

Claim 21 has been amended to incorporate the limitations recited in Claim 5, and to cancel delete "the first circuit and the second circuit are packed by different packaging methods".

**35 U.S.C. 112**

Claims 1-5 and 7 were tentatively rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement. In this regard, the Office Action alleged that, regarding claim 1, the specification does not explain what is mean by the term "on different planes."

Claim 1 has been amended by replacing the term "on different planes" to "on more than one face thereof". Support for the amendment is shown in page 5, lines 23-27 and FIG. 4 of the specification, "The top surface of the cut isolation substrate 20B is a *circuit deposition region 21*, which is deposited on the CPU block, and the side surfaces 26 of the cut isolation substrate 20B contiguous to the circuit deposition region 21 are *substrate-combining regions*".

Accordingly, the 112 rejection has been rendered moot by the amendment to claim 1.

**35 U.S.C. 102(b)**

Claims 1-2, 4, 7 and 21 were tentatively rejected under 35 U.S.C. 102(b) as allegedly anticipated by Kaoth et al. (U.S. 5,963,785). For at least the reasons set forth below, Applicant disagrees and requests reconsideration of the rejection.

Claim 1 recites:

1. A system for integrating circuitry on an isolation layer, comprising:  
*a plurality of isolation substrates, each isolation substrate having a circuit deposition region and a substrate-combining region;*  
a plurality of circuits formed on the circuit deposition regions;  
a plurality of substrate-connecting elements formed to connect the substrate-combining regions; and  
a plurality of electrical connecting elements formed to electrically connect the circuits formed on the different circuit deposition regions, wherein the circuit deposition region contacts the substrate-combining region on more than one face thereof, *and wherein at least two isolation substrates contact at respective substrate-combining regions.*

*(Emphasis added.)*

Kaoth does not teach or suggest a system having at least two isolation substrates, wherein the at least two isolation substrates contact at respective substrate-combining regions. As illustrated in FIG. 3 of Kaoth, the first substrate-combining region of substrate 9 does not contact the second substrate-combining region of substrate 11.

For this reason, claim 1 is allowable over the cited reference. Insofar as claims 2-5 and 7, depend from claim 1 and its related claims, they are also allowable.

Claim 21 recites:

21. A method for integrating a system on an isolation layer, comprising the following steps:  
providing a first isolation substrate including a first circuit deposition region and a first substrate-combining region, and a second isolation substrate including a second circuit deposition region and a second substrate-combining

region, wherein the materials of the first and second isolation substrates are different;

forming a first circuit and a second circuit respectively on the first circuit deposition region and the second circuit deposition region;

forming a plurality of substrate-connecting elements for connecting the first substrate-combining region to the second substrate-combining region; and

forming a plurality of electrical connecting elements to electrically connect the first circuit and the second circuit.

*(Emphasis added.)*

Kaoth does not teach or suggest the materials of the first and second isolation substrates being different, as specifically claimed in claim 21. For at least this reason, claim 21 is allowable over the cited reference.

### Conclusion

For the reasons as described above, all pending claims are now in condition for allowance. Applicant thanks the Examiner for his thorough review of the present application and his allowance of claims 8-20.

Withdrawal of the rejections and allowance of all claims, as now amended, are respectfully requested. Applicant has made every effort to place the present application in condition for allowance. It is therefore earnestly requested that the present application, as a whole, receive favorable consideration and that all of the claims be allowed in their present form.

Should Examiner feel that further discussion of the application and the Amendment is conducive to prosecution and allowance thereof, please do not hesitate to contact the undersigned at the address and telephone listed below.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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**IN THE DRAWINGS:**

FIG. 4 has been amended by replacing the label "22B" on the left side with "24B". Support for the amendment is shown on page 5, lines 20-22 in the specification, "the isolation substrates 20A and 20B are cut along cutting lines 24A and 24B".

**Attachments****Annotated Drawing Sheet****Replacement Drawing Sheet**

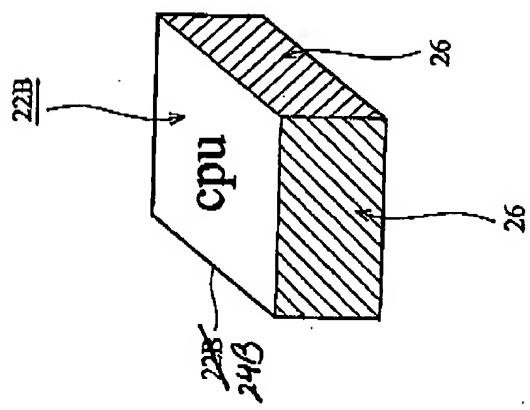
*Annotated Sheet*

FIG. 4

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